CLAIMS

What is claimed is:

1. A semiconductor structure comprising:

a pad area; and

an electrostatic discharge protective device disposed below said pad area.

2. The semiconductor structure as recited in Claim 1 wherein said pad area comprises:

a substrate;

a first layer of metal disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal.;

a second layer of metal disposed above said first layer of metal.

3. The semiconductor structure as recited in Claim 2 further comprising:

a layer of dielectric disposed between said first metal layer and said second metal layer; and

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer.

4. The semiconductor structure as recited in Claim 3 wherein said electrostatic discharge protective device comprises a transistor and a resistance.

5. The semiconductor structure as recited in Claim 4 wherein said via comprises a plurality of individual vias.

6. The semiconductor structure as recited in Claim 5 wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

7. The semiconductor structure as recited in Claim 6 wherein a resistive value of said resistance is fixed during a process for fabricating said semiconductor structure.

8. The semiconductor structure as recited in Claim 7 wherein said resistive value of said resistance is fixed by a method selected from the group consisting essentially of:

setting a particular number for said portion of said plurality of individual vias in parallel;

forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area; and

forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

9. The semiconductor structure as recited in Claim 3 further comprising a subsequent layer of metal between said first and said second metal layers.

10. A pad area apparatus for a semiconductor structure comprising:
a substrate;
a first layer of metal disposed above said substrate;
a second layer of metal disposed over said first layer of metal; and
an electrostatic discharge protective device wherein said electrostatic discharge protective device is disposed within said substrate.

11. The pad area apparatus as recited in Claim 10 further comprising:
a layer of dielectric disposed between said first metal layer and said second metal layer; and
a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer.

12. The pad area apparatus as recited in Claim 11 wherein said electrostatic discharge protective device comprises a transistor and a resistance.

13. The pad area apparatus as recited in Claim 12 wherein said via comprises a plurality of individual vias.

14. The pad area apparatus as recited in Claim 13 wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

15. The pad area apparatus as recited in Claim 14 wherein a resistive value of said resistance is fixed during a process for fabricating said semiconductor structure.

16. The pad area apparatus as recited in Claim 15 wherein said resistive value of said resistance is fixed by a method selected from the group consisting essentially of:
setting a particular number for said portion of said plurality of individual vias in parallel;
forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area; and
forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

17. An electrostatic discharge protective device for a semiconductor structure comprising:
a resistance; and
a transistor disposed within a substrate below a pad area of said semiconductor

structure.

18. The electrostatic discharge protective device as recited in Claim 17 wherein said resistance comprises a plurality of vias of said semiconductor structure, wherein said vias are arranged electrically in parallel, one to another.

19. The electrostatic discharge protective device as recited in Claim 18 wherein a resistive value of said resistance is fixed during a process for fabricating said semiconductor structure.

20. The electrostatic discharge protective device as recited in Claim 19 wherein said resistive value of said resistance is fixed by a method selected from the group consisting essentially of:

setting a particular number for said portion of said plurality of individual vias in parallel;

forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area; and

forming said individual vias comprising said portion of said plurality of individual vias with a particular length.